Naučnoistraživački seminar 1.2.

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Naziv seminara:

"Architectural Trade-Offs in the Design of High-Speed PAM-3 Wireline Transmitters"

ABSTRACT/SAŽETAK

USB4 Version 2.0 is the first generation to adopt Pulse Amplitude Modulation-3 (PAM-3) signaling while increasing the data rate to 40 Gb/s, thus needing PAM-3 transceivers that can satisfy its various requirements. This paper presents the architectural choices and trade-offs in high-speed PAM-3 wireline transmitters. A quarter-rate clocking architecture is adopted to investigate the impact of different driver and Feed-Forward Equalizer (FFE) implementations on complexity, area, and power consumption across varying data rates. Three transmitter architectures are designed and simulated in 22 nm CMOS technology, following the standard as a guideline. Analog and digital FFE implementations are combined with voltage-mode, conventional and DAC driver implementations. All three designs employ a 4-tap FFE as required by the specification. Among them, the DAC-based design achieves the highest energy efficiency and smallest area, whereas the all-analog solution ranks second. The analog driver with digital FFE results in the most power and area consumption.